



Wang, J., Dagan, K., Yuan, X., Wang, W., & Mellor, P. (2019). A Practical Approach for Core Loss Estimation of a High-Current Gapped Inductor in PWM Converters With a User-Friendly Loss Map. *IEEE Transactions on Power Electronics*, 34(6), 5697-5710. <https://doi.org/10.1109/TPEL.2018.2867264>

Peer reviewed version

Link to published version (if available):  
[10.1109/TPEL.2018.2867264](https://doi.org/10.1109/TPEL.2018.2867264)

[Link to publication record in Explore Bristol Research](#)  
PDF-document

This is the author accepted manuscript (AAM). The final published version (version of record) is available online via IEEE at <https://ieeexplore.ieee.org/document/8447285> . Please refer to any applicable terms of use of the publisher.

## University of Bristol - Explore Bristol Research

### General rights

This document is made available in accordance with publisher policies. Please cite only the published version using the reference above. Full terms of use are available:  
<http://www.bristol.ac.uk/red/research-policy/pure/user-guides/ebr-terms/>

# A Practical Approach for Core Loss Estimation of a High-current Gapped Inductor in PWM Converters with a User-friendly Loss Map

Jun Wang, Kfir J. Dagan, Xibo Yuan, Wenbo Wang and Phil Mellor

Department of Electrical and Electronic Engineering, University of Bristol, Bristol, BS8 1UB, United Kingdom

*Corresponding author:*

**Name:** Xibo Yuan

**Postal address:** Department of Electrical and Electronic Engineering, Merchant Venturers Building, Woodland Road, Bristol, BS8 1UB, United Kingdom.

**E-mail:** [xibo.yuan@bristol.ac.uk](mailto:xibo.yuan@bristol.ac.uk)

This paper has not been submitted elsewhere previously.

**Abstract** — Core loss estimation of filter inductors is critical for modelling and optimising high-frequency, high-efficiency and high-density Pulse Width Modulation (PWM) power electronics converters. However, data provided by inductor core manufacturers is insufficient for core loss estimation in PWM converters, particularly in the case of customized gapped inductors. This paper presents a whole process of characterising and estimating the core loss of a customised high-current gapped inductor for PWM converters. To excite the inductor for the B-H loop measurement, a test circuit formed by a half-bridge structure is proposed, which has the ability to compensate the asymmetric rectangular voltage on the inductor caused by the device voltage drops. To overcome the other challenges raised by high excitation current, a discontinuous test procedure, Triple Pulse Test (TPT), is applied to reduce the requirements of the high-current test setup (thermal stress, current-time stress for current probes, capacity of dc sources, etc.). For practical purposes, a user-friendly loss map approach is proposed involving only time-domain and electrical variables to replace magnetic variables to enable straightforward loss mapping process and core loss calculations. Presented experimental results show consistency between the estimated inductor loss and measured values. Overall, the proposed testing approach can be easily implemented on the user's side to develop a loss map of a given inductor. The established core loss map enables the users to accurately and rapidly estimate the core loss of a tested inductor for given PWM waveforms.

**Index Terms** — core loss; B-H loop measurement; loss map; pulse width modulation (PWM); optimisation;

## I. INTRODUCTION

In recent years, high-frequency, high-density and high-efficiency power converters are driven forward by advances in high-speed, low-loss power devices, such as silicon carbide (SiC) and gallium nitride (GaN) based switching devices. In power converters, filter inductors are used to attenuate current ripple and contributes substantially to the total converter volume, weight and power losses. Particularly, filter inductors can contribute to 30~50% of the weight or volume of a typical power converter [1]. Regarding the power loss, the loss characterisation of inductors in general, and their core loss in particular, has been a hot research topic. Accurate estimation of inductor core loss is crucial for the thermal design and optimisation of power converters [2]–[4] in early design stage. It is especially important when considers the high-frequency operation and associated high-frequency core loss with the use of wide-bandgap switching devices. As an example, the inductor studied in the paper is intended for a shunt regulator for aircraft generator application with a targeted switching frequency of over 50 kHz.

Within the context of Pulse Width Modulation (PWM) power converters, there are several challenges in estimating the core loss of filter inductors. **Challenge A:** In a PWM converter, the inductor is exposed to rectangular voltage and triangular current, rather than sinusoidal excitation. However, normally only a limited loss profile generated from sinusoidal excitation can be found in manufacturer's datasheet for one type of core material. Furthermore, Fourier Transformation cannot be applied to decompose the PWM excitation waveform [5]. **Challenge B:** The high frequency triangular current waveform contains a varying, low-frequency dc component. This dc bias factor is also referred as pre-magnetisation, indicating the position of the B-H loop relative to the origin where  $H_0 = 0$ . Pre-magnetisation is reported to have significant impact on the core loss [6]–[9] for particular materials such as Soft Ferrites.

A widely accepted empirical core loss model is the Steinmetz Equation (SE) (1), which indicates the core loss is a function of frequency  $f$  and flux density swing  $\Delta B$ .

$$P = kf^\alpha \Delta B^\beta \quad (1)$$

However, SE is limited in accuracy as the coefficients are only accurate within a certain range of frequency [10], [11]. Moreover, SE is only valid for sinusoidal excitation, which means SE is not directly applicable for the filter inductors driven by

PWM converters.

To overcome Challenge A, Improved Generalised Steinmetz Equation (IGSE) (2) was introduced to calculate the loss of any arbitrary flux waveform [12]–[14].

$$Q = \int_0^T k_i \left( \frac{dB}{dt} \right)^\alpha (\Delta B)^{\beta-\alpha} dt \quad (2)$$

IGSE enables the conversion of SE parameters from sinusoidal excitation to rectangular. The concept of IGSE also includes decomposing a complex waveform into individual B-H loops. It is widely accepted and proven to be accurate. However, as the main drawback, IGSE does not consider the effect of pre-magnetisation [9].

To take the pre-magnetisation effect into account, Challenge B, “loss map” approach was proposed in publications [6]–[8]. This approach relies on experimental B-H loop measurement to construct a core loss profile covering various inductor operating points described by  $H_0$ ,  $\Delta B$  and  $f$ . The measurement configuration of these studies is based on a buck (chopper) converter with rectangular output voltage. The method of utilising the pre-measured loss map to calculate the inductor core loss for PWM inverters is also proposed in [6]–[8], based on decomposing the B-H trajectory into calculable quasi-closed loops. In [15], [16], the loss map calculation method is revised to a half-loop based approach. An approximation method is also proposed for 3-phase PWM converters where there are consecutive segments with  $dB/dt$  changes and the sign not reversed. In [15], [17], based on dynamic B-H loop measurement, Iron Loss Analyser (ILA) is introduced as a system accurately measuring instantaneous core loss (at switching cycles level) and verifies the accuracy of revised loss map. Although, this concept is for real-time experimental evaluation on an operating PWM converter, instead of the estimation of core loss from pre-measured data. As an alternative of loss map, [9] investigated the impact of pre-magnetisation on the SE parameters and presented it in Steinmetz Pre-magnetization Graphs (SPG), with measurements based on a H-bridge converter. However, the accuracy of this approach is limited by the accuracy of original SE parameters. To summarize, establishing a loss map is still the most practical approach to achieve accurate estimation of the core loss.

When it comes to customised inductors (e.g. with gapped cores), the outcomes of the above research are hardly transferable. Most of the previous studies are based on performing B-H loop measurements on toroidal cores, characterising the property of

one type of core material with a relatively low excitation current (e.g.  $<10$  A). However, inductors with gapped cores are widely used for relatively high-current applications (e.g.  $>100$  A) to avoid core saturation. Even if the core loss profile of a magnetic material is given, it still cannot be applied on gapped cores directly. For example, the  $H$  axis of the loss map for a gapped core must be rescaled, since the operational range of  $H$  is extended. Additionally, a gapped core potentially comes with excessive gap loss as reported in [18], which is essentially eddy current losses concentrated around the airgap. This is not predictable from the loss data measured from toroidal core and directly associated with the physical shape of the core, especially the airgap length. But these effects can still be evaluated as B-H loop measurement covers all the core loss components including hysteresis loss and eddy current loss [19], [20]. Furthermore, core loss is very sensitive to the actual physical property of individual inductor cores. For laminated cores, the thickness and alignments of the laminations could drift from the designed form unpredictably from batch to batch. It is also pointed out in [21] that “Characterising a specific core or a specific wound component is better (more accurate, easier to use) than characterising a material”. Additionally, the effect of pre-magnetisation is normally not assessed by the supplier of the core material. To count in this effect for better accuracy, additional experimental evaluation is required. Therefore, evaluation of a specific inductor on the user’s side is necessary to achieve better accuracy.

To evaluate a specific, customised inductor, new challenges arise. Consider a specific high-current gapped inductor is given with the structure unalterable (e.g. potted/housed). To meet the designed operating point of  $H$ , it is not feasible to reduce the amplitude of excitation current by increasing the number of turns as the windings are fixed. In this case, the inductor loss mapping process requires high excitation current. This high current can result in unwanted temperature rise, a large dc current-time product for current probes and asymmetric excitation voltage due to significant voltage drop on power devices.

In addition, the loss map approach developed in previous studies is not straightforward for practical purposes. Firstly, it is normally employed in the form of a three-dimensional look-up table [15], [22] that is difficult to be presented or utilised. Secondly, the variables in loss map is normally in magnetic form while it is more common to use electrical and time-domain variables in the context of power electronics. The translation between these variables complicates the loss mapping process and core loss calculations. Additionally, the translation involves the effective dimensions of the core. In some cases this information

is not available (e.g. not provided for housed inductor), or not accurate, which could affect the accuracy of the core loss calculation [20].

Therefore, this study intends to present **a whole process of characterising and estimating the core loss of a customised, high-current, gapped inductor for PWM operations**. It covers from experimentally establishing a loss map to utilizing the loss map to estimate the inductor's core loss in PWM converters. The main contributions of this paper are given as follows. To excite the inductor-under-test, **a new test circuit is proposed, which is based on a half-bridge structure and enables the compensation of the asymmetric rectangular voltage caused by the device voltage drops**. To overcome the other challenges raised by high excitation current (e.g. 100 A), a discontinuous testing procedure, Triple Pulse Test (TPT), is applied in this study. The idea of Triple Pulse Test is to run necessary cycles only and avoid unnecessary operations. Similar ideas were discussed in previous studies, such as in [9] and [23]. This study further reveals the significant benefits of TPT in the context of testing the core loss with high excitation current. TPT does not require the full continuous operation capability of the converter and inductor. It reduces the requirements of the test setup (thermal stress, current-time stress for current probes, current capacity of dc sources, etc.) and enables a fast evaluation. Additionally, Triple Pulse Test is analogous to the Double Pulse Test (DPT) in characterising switching loss of power devices. As such, it can be easily understood and adopted by a power electronics engineer who is familiar with DPT. Furthermore, a loss map calculation approach is presented to utilise the pre-built loss profile to calculate/estimate the core loss of the tested inductor when operating in a PWM converter. **A user-friendly loss map and core loss calculation method involving only time-domain and electrical variables**, which replaces the conventional magnetic variables, has been proposed to enable straightforward loss mapping process and simplified core loss estimation. An experimental evaluation of the proposed approach is conducted on a real PWM converter. This paper is presented in three steps: (1) Core loss measurement (2) Establish a loss map and utilize it to estimate the core loss for PWM operations (3) Experimental evaluation.

## II. CORE LOSS MEASUREMENT

### A. *B-H Loop Measurement*

As mentioned in the previous section, B-H loop measurements have been used in many papers for the evaluation of core loss [8], [9], [22]. This approach measures the core loss of an inductor with the copper loss excluded. To perform B-H loop

measurement, the inductor is equipped with two windings: a primary winding for excitation current and a secondary winding to sense core flux as shown in Fig. 1. By measuring the excitation current  $I$  on the primary side and the open-circuit voltage  $U_{Lsec}$  on the secondary side, the magnetic field  $H$  and flux density  $B$  can be found by the relationships expressed by (3) and (4)

$$B(t) = \frac{1}{N_2 A_e} \int_0^T U_{Lsec}(t) dt \quad (3)$$

$$H(t) = \frac{N_1 \cdot I(t)}{l_e} \quad (4)$$

Where  $N_1$  and  $N_2$  are the numbers of turns of the primary winding and secondary winding, respectively;  $A_e$  is the effective cross-section area of the core;  $l_e$  is the effective length of magnetic path.

Then the core loss is obtained from (5) by integrating the product of the secondary voltage and primary current, with the turns ratio accounted. Note that in (5), the geometry parameters of the core  $A_e$  and  $l_e$  are irrelevant regarding the measured total core loss in the form of energy.

$$Q = A_e l_e \int H dB = \frac{N_1}{N_2} \int_0^T I(t) \cdot U_{Lsec}(t) dt \quad (5)$$

Fig. 1 shows a basic schematic of a B-H loop measurement test rig, formed by a dc power supply, a power converter, the inductor-under-test, voltage and current probes and a digital oscilloscope. A typical voltage-current waveform for B-H loop test is shown in Fig. 2, with square-wave excitation voltage. The curvy shape of the current, instead of a triangular shape, is caused by the magnetization process [8]. In practice, the accuracy of B-H loop measurement is sensitive to the phase discrepancy between the measured voltage and current [8], [20], [24]. Therefore, the phase differences of the probes must be carefully calibrated.

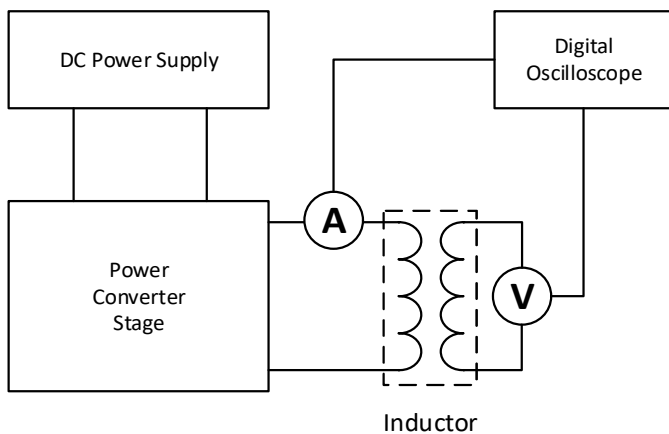


Fig. 1. Overview of the test system

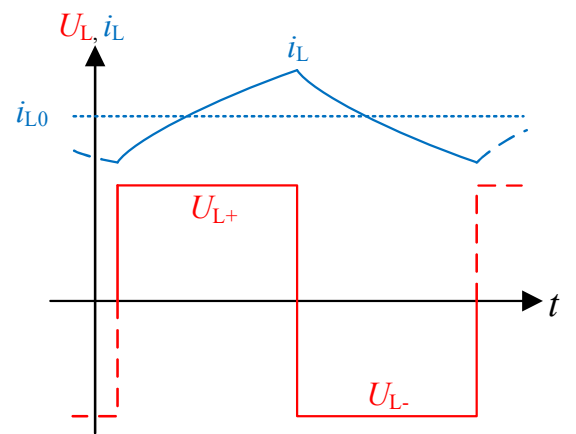
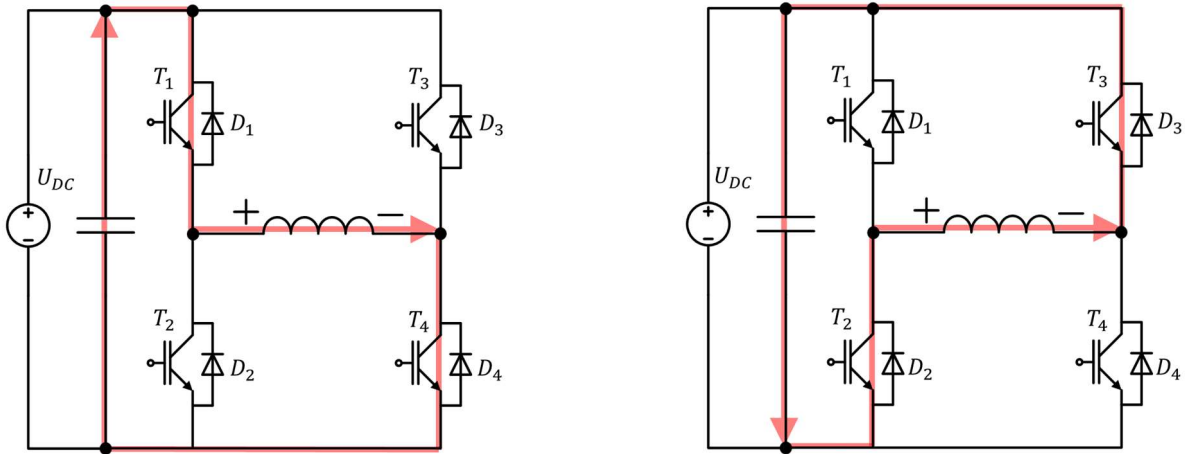


Fig. 2. Typical voltage/current waveforms of the inductor for B-H loop measurement with dc-biased current

### B. Power Converter Configuration

For the power converter stage in Fig. 1, a common configuration is a buck converter [8], [9]. However, a buck converter can only evaluate the operating points with the current flowing in one direction. In PWM converters, there are operating points of the inductor with the current crossing both directions within one switching cycle. Therefore, this topology is not ideal for the evaluation of the whole operating region of the inductor in a PWM converter.

As an option with bidirectional conduction capability, a test circuit formed by a H-bridge structure is shown in Fig. 3, which is also a common configuration in studies such as [25], [26]. However, for the scope of this study, H-bridge configuration features a significant drawback. For a pre-built high-power gapped inductor, a high excitation current must be driven into the inductor, especially for the operating points with high  $H_0$ . When a high current is fed into the inductor, the voltage drops across the power devices at the power converter stage becomes significant. When a dc-biased current as shown in Fig. 2 is driven into the inductor, an asymmetric square-wave voltage will cross the inductor, with unequal amplitudes  $U_{L+}$  and  $|U_{L-}|$ . In the positive cycle shown in Fig. 3(a), the inductor current is drawn from the dc-link and flows through T1, the inductor and T4. The inductor voltage  $U_{L+}$  can be expressed by (6). In the negative cycle shown in Fig. 3(b), the inductor current flows through diodes D2, D3 and charges the dc-link capacitor. The inductor voltage  $U_{L-}$  in this case can be expressed by (7).



(a) positive cycle with dc-biased current (charging inductor) (b) negative cycle with dc-biased current (discharging inductor)

Fig. 3. H-bridge test circuit

$$U_{L+} = U_{DC} - 2U_{IGBT} \quad (6)$$

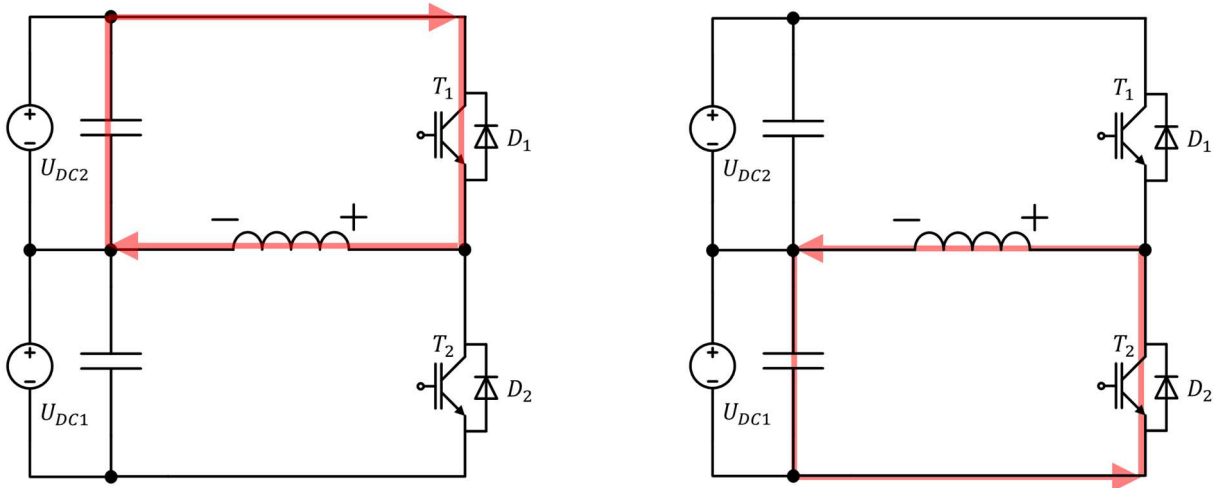
$$U_{L-} = -(U_{DC} + 2U_{Diode}) \quad (7)$$

Where,  $U_{DC}$  is the converter dc-link voltage,  $U_{IGBT}$  is the IGBT forward voltage drop,  $U_{Diode}$  is the diode forward voltage drop.



Taking an IGBT power module SKiM301TML112E4B (1200V, 300A) as an example, given a current of 100 A,  $U_{IGBT}$  is around 1.5 volts and  $U_{Diode}$  is around 1.8 volts according to the datasheet. Assuming  $U_{DC} = 50$  V, theoretically the voltage drops would lead to  $U_{L+} = 47$  V and  $U_{L-} = -53.6$  V following (6) and (7), which is a 6.6 V bias in total. This asymmetry will prevent the measured B-H trajectory from forming a closed loop and have unneglectable impact on the measured core loss. Unclosed B-H loop will compromise an important assumption to be elaborated in the next section, where it assumes the positive half cycle and the negative half cycle of a B-H loop each consumes equal energies.

In order to achieve more reliable and accurate measurements, this asymmetry caused by device voltage drops must be mitigated. Therefore, an alternative test circuit for the power stage is proposed in this paper as shown in Fig. 4. This test circuit comprises a half bridge structure with two tunable dc power sources ( $U_{DC1}$  and  $U_{DC2}$ ) and two capacitors in series to form the dc-link. The inductor-under-test is placed between the output port of the half bridge and the neutral point of the dc-link.



(a) positive cycle (charging inductor) with dc-biased current (b) negative cycle (discharging inductor) with dc-biased current

Fig. 4. Half bridge test circuit

This configuration brings extra degree of freedom: the two dc-link voltage supplies can be adjusted to compensate the asymmetric voltage drops. In the positive cycle, the current is drawn from the pre-charged capacitor with voltage  $U_{DC2}$ , flows through  $T1$  and charges the inductor, as shown in Fig. 4(a). In this case the inductor voltage  $U_{L+}$  is expressed by (8). Fig. 4 (b) shows the current in the negative cycle, where the inductor voltage  $U_{L-}$  is expressed by (9).

$$U_{L+} = U_{DC2} - U_{IGBT} \quad (8)$$

$$U_{L-} = -(U_{DC1} + U_{Diode}) \quad (9)$$

By tuning the output voltages of the two dc power supplies,  $U_{DC2}$  and  $U_{DC1}$ , the inductor voltages  $U_{L+}$  and  $|U_{L-}|$  can be compensated to equal. For example, if  $U_{IGBT} = 1.5$  V and  $U_{Diode} = 1.8$  V,  $U_{DC2}$  and  $U_{DC1}$  can be set as 51.5 V and 48.2 V respectively to achieve  $U_{L+} = |U_{L-}| = 50$  V. In practice, the voltage drops on the power devices ( $U_{IGBT}$  and  $U_{Diode}$ ) may deviate from what has been given the datasheet. The parasitic resistance of the test circuit also contributes to the voltage drops. In this case, the values of supply voltages  $U_{DC2}/U_{DC1}$  are empirically determined by tuning  $U_{DC2}/U_{DC1}$  and measuring  $U_{L+}/U_{L-}$  until the inductor voltage reaches aimed symmetric rectangular for each operating point.

### C. Test Procedure – Triple Pulse Test

The goal of the B-H loop measurement is to measure the area of a closed B-H loop given the operating point described by  $H_0$ ,  $\Delta B$  and  $dB/dt$ . To overcome the challenges introduced by high excitation current, a discontinuous measurement procedure is applied in this study. The idea of this approach is applying limited pulses (triple pulses) to reach the desired B-H loop and avoid further unnecessary operation, which leads to a test waveform that is similar to the saturation property test in [23]. For the scope of this study, where a large peak current is required (e.g. 100 A), this triple-pulse-test (TPT) holds the following merits:

(1) Does not require a dc power supply with the capacity of supplying a large continuous current. As this is a relatively fast and short transition (e.g.  $< 200$   $\mu$ s), the current required in this process is mainly drawn from the dc-link capacitors.

(2) Significant temperature rise is avoided due to little heat generated from this process.

(3) In the case where the current is measured by current probes, the dc current-time product  $I \cdot t$  (in  $A \cdot \mu$ s) in the process must not exceed the allowable range, so that they would not saturate (reach non-linear operation region). Taking current probe N2781B as an example, the maximum allowable non-continuous current-time product is stated at 15000  $A \cdot \mu$ s. This means that if the dc biased current is 100 A, the time duration of the whole testing process is limited to  $< 150$   $\mu$ s. A large dc current-time product is avoided in the proposed process as limited pulse cycles are supplied.

The process of the TPT approach is illustrated in Fig. 5: Stage I, an initial pulse is supplied to build up the desired pre-magnetisation  $H_0$ ; Stage II, several cycles with desired flux density swing are supplied to force the B-H trajectory into aimed steady state; Stage III, the B-H trajectory stabilises and forms the desired B-H loop; Stage IV, the power devices are all turned-

off, and the energy stored in the inductor releases through the free-wheeling diodes, which leads to the current dropping back to zero at the end of this process. The B-H loop of interest is obtained in Stage III. The turn-on and turn-off delay of the power devices is compensated in the generation of gate signals to ensure the ON duration  $T_{2+}$  equals to the OFF duration  $T_{2-}$ .

By experimental observations, the B-H trajectory stabilises at the aimed B-H loop as of the second or the third pulse cycle for most of the operating points. An example of the B-H trajectory measured from one discontinuous measurement is shown in Fig. 6, where the blue loop is the second pulse cycle and the red loop is the third pulse cycle. The dashed line shows the pre-magnetisation process and the de-magnetisation process. It is visible that the blue and red loops are self-closed and similar in shape and area. Consecutive pulses would only repeat the trajectory of the third loop and result in the same close-loop area. Therefore, in the following study, the third B-H loop cycle is captured for core loss calculation and the proposed test approach is therefore called TPT. Note TPT procedure should not make any differences compared to the B-H loop measurement used in other studies, since it only intends to measure the first steady-state B-H loop and avoid further unnecessary operations.

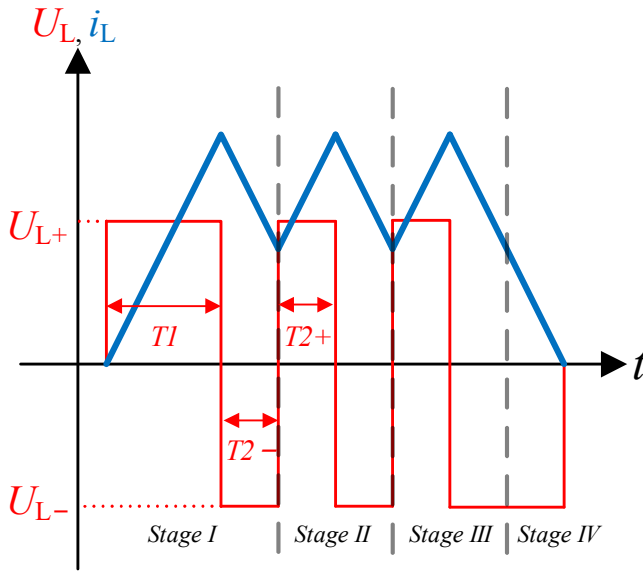


Fig. 5. Inductor current/voltage waveform of Triple Pulse Test

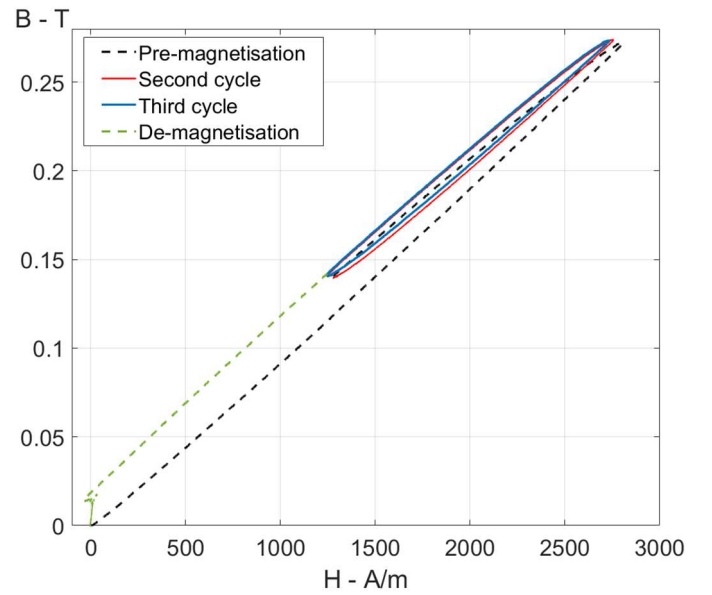


Fig. 6. Example of measured B-H trajectory from TPT ( $H_0 \approx 2000$  A/m,  $\Delta B \approx 130$  mT)

The concept of this proposed TPT approach is analogous to the Double Pulse Test (DPT) [27], which is widely used for evaluating the switching loss of a semiconductor device (e.g. IGBT or MOSFET). Therefore, it is relatively easy for engineers who are familiar with DPT to adopt the TPT approach for inductor core loss characterisation. A comparison between these two procedures is presented in Table I.

TABLE I. COMPARISON BETWEEN DPT AND TPT

	DPT for power devices	TPT for inductors
Initialization pulse(s)	To build up the switching current $I_0$	To build up pre-magnetisation $H_0$
Pulse of interest	Rising edge for turn-on loss Falling edge for turn-off loss	A closed B-H loop with dc-bias $H_0$ and flux density swing $\Delta B$
Voltage $U$	Switching voltage $U_{sw}$	Flux density change rate $dB/dt$
$TI$	Determined by $U_{sw}$ , $I_0$	Determined by $dB/dt$ , $H_0$
$T2- / T2+$	Not relevant	Determined by $dB/dt$ and $\Delta B$

#### D. Test Setup

A customised inductor-under-test is shown in Fig. 7, with the parameters listed in Table II. It is formed by EE cores (double E-core) made from Cobalt Iron (CoFe) laminations. The rated current of the inductor is 80 Arms. This inductor is designed as the output current ripple filter of a high-power shunt regulator system.

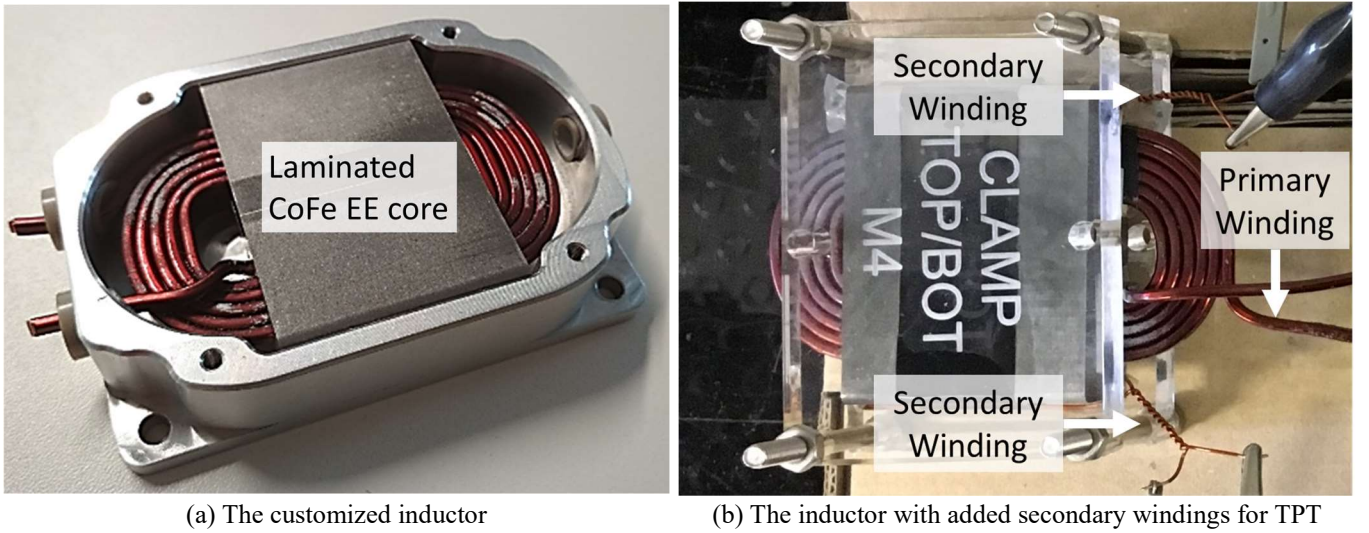


Fig. 7. Inductor under test

The airgap is at the central leg of the EE core with a length  $l_g$  of 0.52 mm. The copper windings are spaced away from the central leg for larger than four times  $l_g$  to avoid the fringing flux effect.

TABLE II. SPECIFICATIONS OF THE INDUCTOR UNDER TEST

Core Material	VACOFLUX48 0.01mm (laminated Cobalt Iron)	Winding	1.9 * 2.8 mm rectangular copper
Air gap length $l_g$	0.52mm	Rated current	80 Arms
Shape	EE cores	Rated Inductance	36 uH
N1	6 turns	N2	3 turns

As illustrated in Fig. 7 and in Table II, the primary winding (main inductor winding) has 6 turns. Two secondary windings, with three turns for each, are fitted for TPT at two side legs of the inductor to capture the flux on both sides in case of asymmetric flux distribution. In this case, the relationship between the two measured secondary voltages and the total flux density change is

shown in equation (10)

$$U_{Lsec1} + U_{Lsec2} = N_2 \frac{d\Phi_1}{dt} + N_2 \frac{d\Phi_2}{dt} = N_2 \frac{d\Phi}{dt} = N_2 A_e \frac{dB}{dt} = U_{Lsec} \quad (10)$$

A test rig is built and shown in Fig. 8, formed by dc-link, power converter and measurement probes.

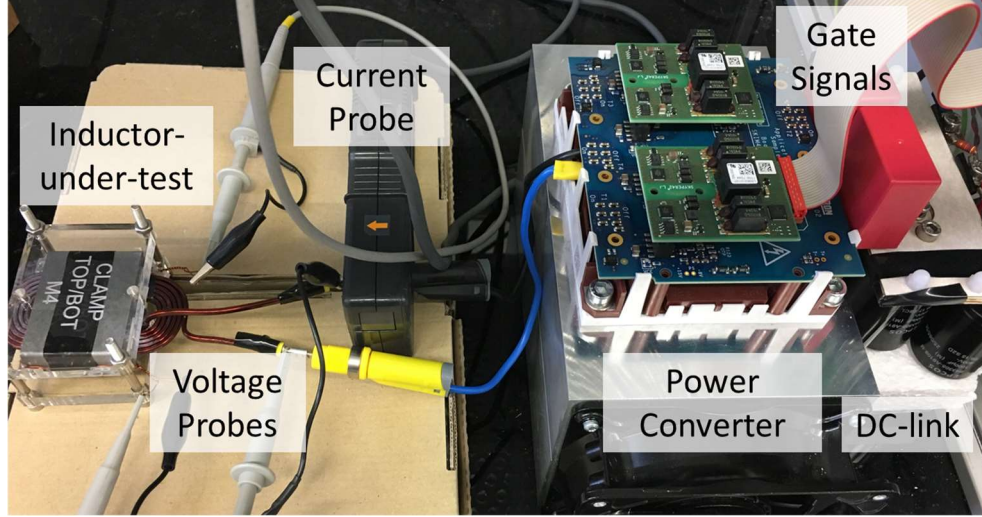


Fig. 8. Test rig

The signals are measured by high-bandwidth voltage and current probes shown in Table III and fed to a digital oscilloscope.

The phase discrepancy between the voltage and current probes is aligned by offline de-skew.

TABLE III. INSTRUMENTS AND COMPONENTS IN THE TEST RIG

<b>Power supply</b>	Elektro-Automatik TS 8000 T	<b>Power module</b>	Semikron SKiM301TMLI12E4B
<b>Voltage probe</b>	Keysight N2862B (150 MHz)	<b>Current probe</b>	Keysight N2781B (10MHz)
<b>Digital Oscilloscope</b>	MSO-X 3054A (500 MHz, 4 GSa/s)		

### III. LOSS MAP APPROACH

The above presented test rig and procedure enables the core loss measurement of the inductor. The following section elaborates how to establish a loss map based on finite measurements in order to estimate the core loss for PWM operations.

#### A. Loss Map

As mentioned in the introduction, a loss map needs to be built up experimentally for a given inductor, which is a database of core loss that covers all possible operating points. For this purpose, the variables describing one operating point must be identified first. There are three known variables describing a closed B-H loop excited by symmetric square-wave excitation (regardless of the operating temperature):

- (1) Flux density change rate  $|dB/dt|$ . This variable is convertible to frequency  $f$  for repetitive symmetric excitation as appeared in a number of papers [22]. However, for an instantaneous point on the B-H trajectory, it is more suitable to refer this variable as  $|dB/dt|$  rather than frequency. In the context of power electronics,  $|dB/dt|$  is proportional to the amplitude of the applied square-wave voltage on the inductor. This is also pointed out in [28] and indicated in Improved Generalised Steinmetz Equation (9).
- (2) Flux density swing  $\Delta B$ .
- (3) Pre-magnetisation/dc-bias of the magnetic field  $H_0$ .

Therefore, a loss map, a database of core loss, is a function of the above three variables, as expressed in (11). A loss map produced from finite discrete measurements can be utilized as a three-dimensional lookup table with interpolations or fitted curves/surfaces with mathematical expressions.

$$Q = f\left(\left|\frac{dB}{dt}\right|, \Delta B, H_0\right) \quad (11)$$

For the first variable, it is reported that the effect of  $|dB/dt|$  regarding core loss is independent from the other two variables ([9], [28], [29]). The correlation between the core loss and  $dB/dt$  is in the form as equation (12) as indicated in IGSE. Therefore, factor  $dB/dt$  can be assessed independently by only one set of data (i.e. fixed  $\Delta B$  and  $H_0$ ) to determine the coefficient  $\alpha$ . This simplifies the loss mapping process by one dimension.

$$Q \propto \left(\left|\frac{dB}{dt}\right|\right)^\alpha \quad (12)$$

According to previous studies, the other two variables,  $\Delta B$  and  $H_0$ , are coupled factors with respect to the core loss. Therefore, given a fixed  $dB/dt$ , data sets covering the possible operating region of interest formed by various  $\Delta B$  and  $H_0$  need be evaluated as shown in (13).

$$Q = \left(\left|\frac{dB}{dt}\right|\right)^\alpha \cdot f'(\Delta B, H_0) \quad (13)$$

To establish the loss map, the inductor-under-test is characterised experimentally using the test rig shown in Fig. 8. The core loss measurement is conducted with the presented TPT procedure. The measured data of secondary voltage and primary current is then processed in Matlab following expressions (3)-(5).

The loss mapping process is conducted in two steps. Firstly, keeping  $|dB/dt|$  ( $U_{L+}$  and  $U_{L-}$ ) fixed, operating points with various  $\Delta B$  and  $H_0$  are tested. The results are shown in in Fig. 9(a) in the form of a surface with thin spine interpolation. It shows that the relationship between  $H_0$ ,  $\Delta B$  and core loss  $Q$  is complex and difficult to be fitted with a generalised expression. This finding is similar to the previous studies [9]. Secondly, to determine the dependency of  $|dB/dt|$ , a set of points with constant  $\Delta B$  and  $H_0$  is realized by varying  $|dB/dt|$ . The results are shown in Fig. 9(b). Curve fitting is performed on this set of data to determine the parameter  $\alpha$  in (13). As can be seen from Fig. 9(b), the measured data is well fitted with a power equation as in (12).

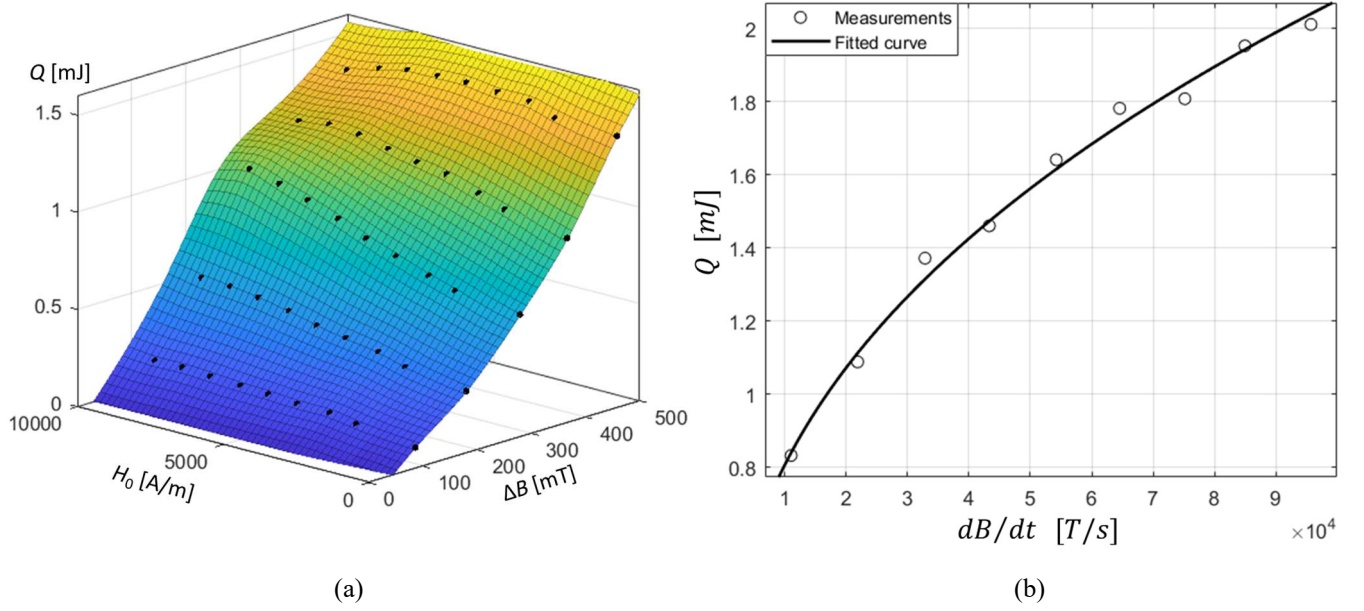


Fig. 9. Loss map (a)  $Q$  vs.  $\Delta B$ ,  $H_0$  ( $dB/dt = 21840$  T/s) (b)  $Q$  vs.  $dB/dt$  ( $\Delta B = 365$  mT and  $H_0 = 4000$  A/m)

### B. Core Loss Calculation for PWM operations

The loss map developed above is based on closed B-H loops excited by symmetric square wave (duty cycle equals 50%,  $U_{L+} = |U_{L-}|$ ) as shown in Fig. 2. However, for filter inductors in PWM converters, it is more common to witness an asymmetric quasi-square-wave excitation  $U_L(t)$  in each switching window as shown in Fig. 10, where  $U_{ab} \neq |U_{bc}|$ ,  $T_{ab} \neq T_{bc}$ . The non-50-to-50 duty cycle is due to the Pulse Width Modulation. The unequal  $U_{ab}$  and  $|U_{bc}|$  are caused by the fundamental-frequency sinusoidal dc-bias. To calculate the core loss for this type of waveform utilizing the loss map produced, an approach combining the piecewise concept of IGSE [5], [11], [13], [14] and revised loss map calculation [15], [16], [22] is adopted in this study. The idea of this approach is decomposing a given PWM waveform into calculable half-loop segments. One half-loop segment is either the positive half with  $dB/dt > 0$  (red part in Fig. 11) or the negative half with  $dB/dt < 0$  (blue part in Fig. 11) of a B-H loop.



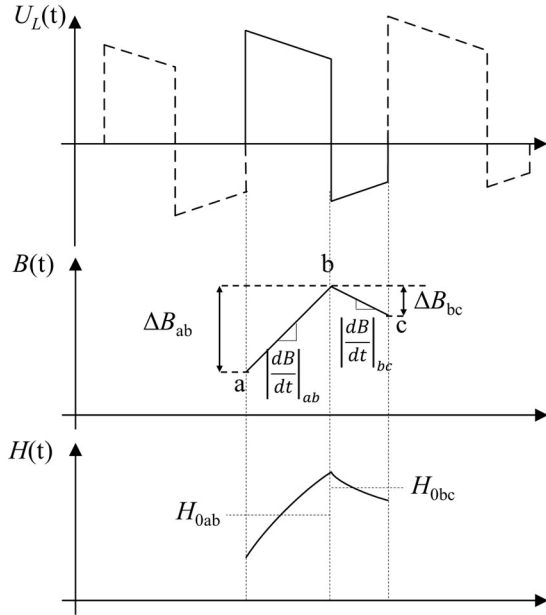


Fig. 10. Typical waveforms of the filter inductor with a single-phase two-level PWM converter

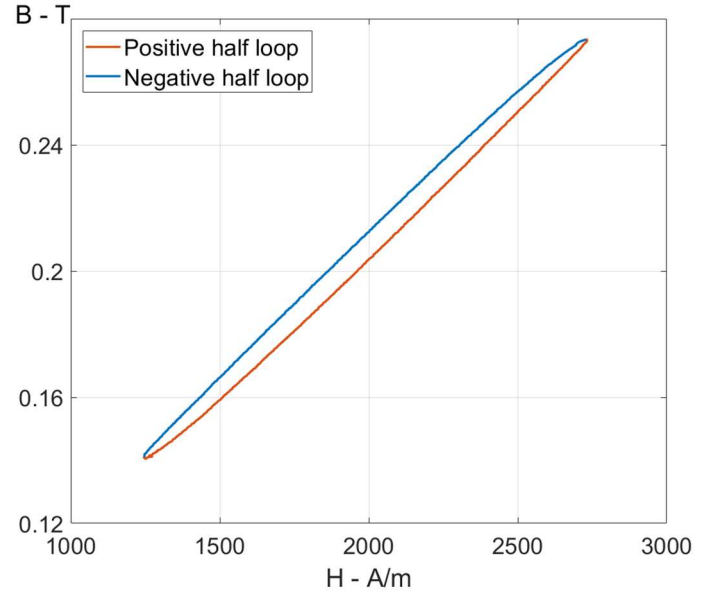


Fig. 11. Example of a measured B-H loop excited by symmetric square wave with pre-magnetisation ( $H_0 \approx 2000$  A/m,  $\Delta B \approx 130$  mT)

Three important assumptions are made in this approach:

- (1) The start/end points of one half-loop segment are considered at the moments where the polarity of  $dB/dt$  reverses, e.g. point  $a$  and point  $b$  shown in Fig. 10. In the case of varying  $|dB/dt|$  within one segment, the average value (e.g.  $\Delta B_{ab}/T_{ab}$ ) is treated as the equivalent  $|dB/dt|$ . This is similar to the linear approximation (revised loss map approach) in [15], [22], [30], which has been proven to be accurate.
- (2) Considering the core loss is instantaneous, it is assumed that the positive half ( $dB/dt > 0$ ) and the negative half ( $dB/dt < 0$ ) each consumes 50% of the total energy loss of the closed B-H loop with symmetric excitation [15], [20], [30]. For example, the core loss of segment  $ab$  is obtained by equation (14) from the loss map described by (11).

$$Q_{ab} = \frac{1}{2} \cdot f \left( \left| \frac{dB}{dt} \right|_{ab}, \Delta B_{ab}, H_{0ab} \right) \quad (14)$$

- (3) The “relaxation effect” [11], [21], [26], [31], [32] is not considered, because the typical voltage applied on the filter inductors of PWM converters does not experience any periods with constant flux density ( $U_L = 0$ ) due to the varying fundamental-frequency dc-bias.

Based on the above assumptions, a given quasi-square-wave excitation can be decomposed into  $n$  pieces of half-loop segments. Then the energy loss for each segment can be found individually through the loss map. The total power loss of a given



waveform can be calculated by adding up the power losses of all half-loop segments that forms this waveform as in (15).

$$Q_{total} = \sum_{n=1}^n Q_{(n)} \quad (15)$$

In this way, a switching window with non-50-to-50 duty cycle is decomposed into two half-loop segments, which are corresponding to a wider pulse and a narrower pulse. For instance, given the waveform  $a$  to  $c$  in Fig. 10, the waveform is decomposed into wider segment  $ab$  and narrower segment  $bc$ . For segment  $ab$ , three descriptive variables of it,  $\Delta B_{ab}$ ,  $H_{0ab}$  and  $|dB/dt|_{ab}$ , are fed into the loss map to obtain the core loss  $Q_{ab}$  by (14). The narrower segment  $bc$  is equivalent to half a symmetric full cycle with higher frequency  $1/T_{bc}$  (i.e. higher  $dB/dt$ ) in the loss map. The total core loss from point  $a$  to  $c$  equals to the sum of  $Q_{ab}$  and  $Q_{bc}$ . For more complex waveforms, such as PWM waveforms, they only need to be decomposed into finite piecewise half-loop segments following this approach. Note in Fig. 9(b), the top right tested point reaches 365 mT with a speed of  $9.6e4$  T/s, which is equivalent to a 130 kHz symmetric positive-negative cycle. Therefore, the testing in this work equivalently covered a wide range of frequency. Theoretically, the presented approach can be extended to any frequency if the hardware allows.

### C. User-Friendly Loss Map and Core Loss Calculation

As mentioned previously, this study aims at utilizing a pre-measured loss map such as those shown in Fig.9 to estimate the core loss in a PWM converter, which is, specifically, to calculate the inductor core loss over a fundamental cycle of a PWM waveform. In this case, the steady-state PWM waveforms on the inductor must be provided and processed to be fed into the loss map, and the steady-state PWM waveforms are normally generated by simulations. These waveforms are generated in the form of the inductor current  $I$  and voltage  $U_L$ . However the conventional loss map used in previous studies (e.g. [8], [9]) requires  $H/B$  waveforms in time-domain, as shown in Fig. 9. Referring to equations (3) and (4), to translate the voltage/current waveforms into  $H/B$  waveforms, it involves the geometry parameters of the inductor core, which introduces additional complexity and uncertainty. It has been pointed out in [20] that the inaccuracy of the effective dimensions of the core may lead to substantial errors in loss calculation, if the loss map is supplied in the form of loss density (e.g. J/m<sup>3</sup>). In some cases, the accurate geometry information is not available, e.g. housed inductors. Therefore, it is motivated to convert the whole process into electrical and time-domain variables rather than  $H/B$  based, which is more user-friendly in practice.

Fig. 12 shows one sample segment in time-domain. Two consecutive zero-crossings of the inductor primary voltage  $U_{Lpri}$  are detected as the start/end point of one half-loop segment. Corresponding to  $H_0$ , the average current  $I_0$  of this segment is measured, as in (16). Corresponding to  $\Delta B$  and  $dB/dt$  as shown in (17) and (18), time duration  $T_{ab}$  and average primary inductor voltage  $\bar{U}_{Lpri}$  are measured.

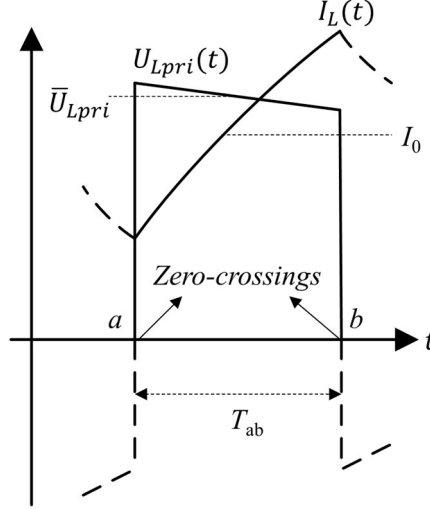


Fig. 12. Example of half-loop segment  $ab$  with only electrical and time-domain measurements

$$H_0 = \frac{1}{T_{ab}} \cdot \frac{N_1}{l_e} \int_a^b i(t) dt = I_0 \cdot \frac{N_1}{l_e} \quad (16)$$

$$\frac{dB}{dt} = \frac{1}{T_{ab}} \frac{1}{N_2 A_e} \int_a^b U_{Lsec}(t) dt = \bar{U}_{Lpri} \cdot \frac{1}{N_1 A_e} \quad (17)$$

$$\Delta B = \frac{1}{N_2 A_e} \int_a^b U_{Lsec}(t) dt = \bar{U}_{Lpri} \cdot T_{ab} \cdot \frac{1}{N_1 A_e} \quad (18)$$

In this way, the loss map generated can be converted to the form expressed as (19) with electrical and time-domain variables.

$$Q = g(\bar{U}_{Lpri}, \bar{U}_{Lpri} T_{ab}, I_0) \quad (19)$$

It becomes a look-up table with three inputs: average inductor voltage  $\bar{U}_{Lpri}$ , volt-time product  $\bar{U}_{Lpri} T$  and dc-biased current  $I_0$ . The output  $Q$  is the energy loss of a half-loop segment in  $mJ$ . This form of loss map will not only enable more straightforward core loss calculation, but also simplify the loss mapping process, compared to magnetic-domain loss map shown in Fig. 9. The electrical and time-domain parameters (pulse width and height) required in the Triple Pulse Test can be obtained directly give an aimed operating point on the user-friendly loss map, without translating from magnetic domain.

Furthermore, it is also difficult to illustrate the conventional three-dimensional loss map in surfaces for practical purposes, e.g. to present in a datasheet. Therefore, a core loss profile presented in curves is proposed in this paper as follows. Fig. 13(a)

shows the energy loss in  $mJ$  versus the biased current  $I_0$ , with various sets of volt-time product in  $V \cdot \mu s$  (corresponding to  $\Delta B$ ). It is noticeable that the effect of  $I_0$  is not identical for each set of data with the same volt-time product. But for each individual set, it can be well fitted with a cubic function. Operating points in between the curves can be obtained by interpolation. Converted from Fig. 9(b), Fig. 13(b) illustrates the core loss normalized to 50 V with respect to the inductor voltage  $U_L$ , as the testing voltage for Fig. 13(a) is  $\pm 50$  V. These curves shown in Fig.13 can be printed on datasheets by the manufacturers of inductors.

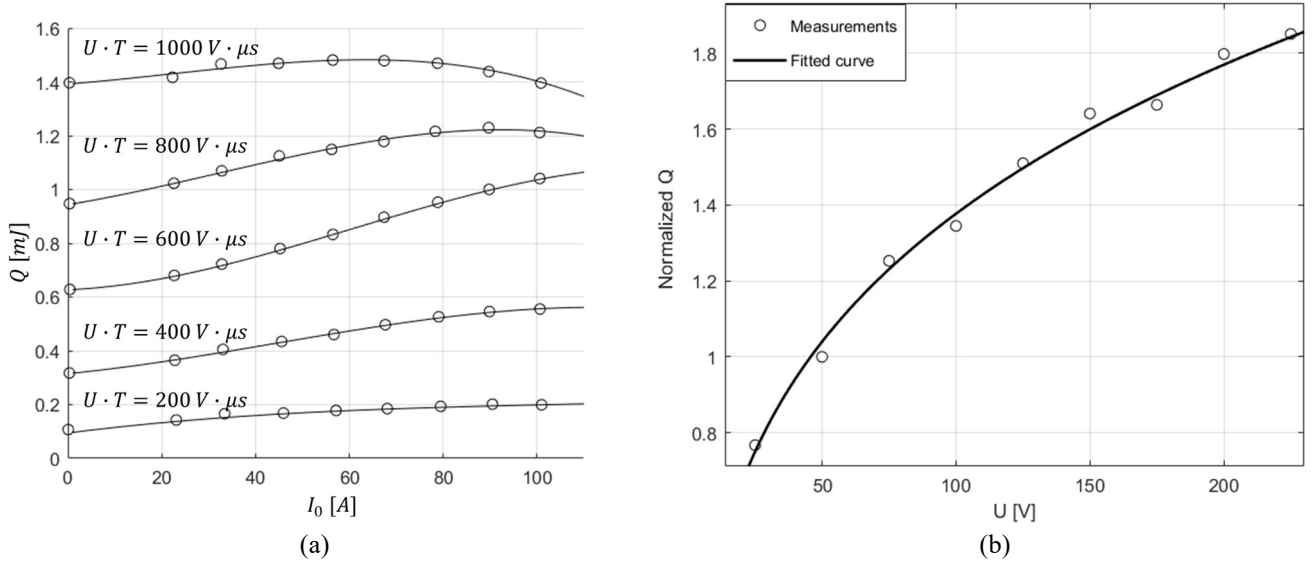


Fig. 13. User-friendly loss map (a)  $Q$  vs.  $U_L \cdot T$  and  $I_0$  ( $U = 50$  V) (b)  $Q$  vs.  $U_L$  normalized to 50 V

To summarize, the energy of a half-loop segment can be found from a user-friendly loss map by two steps: (A) Input  $U_L \cdot T$  and  $I_0$  to Fig. 13(a) to find the energy in mJ. (B) Input  $U_L$  to Fig. 13(b) to scale the energy with respect to the testing voltage  $\pm 50$  V. The core loss calculation flow following the above description is shown in Fig. 14.

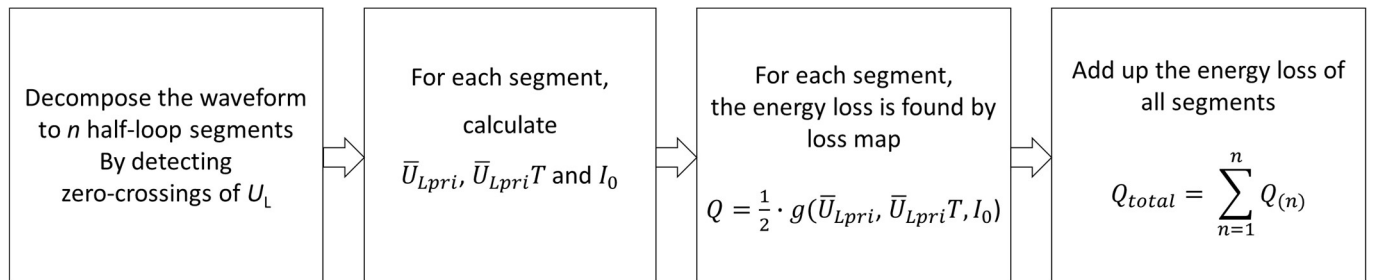


Fig. 14. Core loss calculation flow for a given voltage/current waveform

In the case of a PWM waveform, it is decomposed into half-loop segments ( $n = 2 \cdot f_{sw} / f_0$ ) for each fundamental cycle, and the energy loss of each single segment is calculated and summed up. As an example, consider a single-phase two-level converter is outputting a PWM waveform with 50 Hz fundamental frequency and 20 kHz switching frequency with a modulation index less than 1. In this case, 400 positive and 400 negative half-loop segments can be extracted from one fundamental cycle. This

calculation flow can be easily implemented as an automated block either in simulation models or experimental evaluation, once the loss map of a specific inductor is pre-built with the boundaries covering possible operating plane.

#### IV. EXPERIMENTAL EVALUATION

To implement and evaluate the proposed loss map approach outlined above, an experiment was designed and conducted. A test rig was designed to feed the inductor-under-test with PWM excitation. As shown in Fig. 15, the circuit is formed by a two-level converter with RLC load. The output of the power converter is filtered by the LC filter and applies on the load resistor.

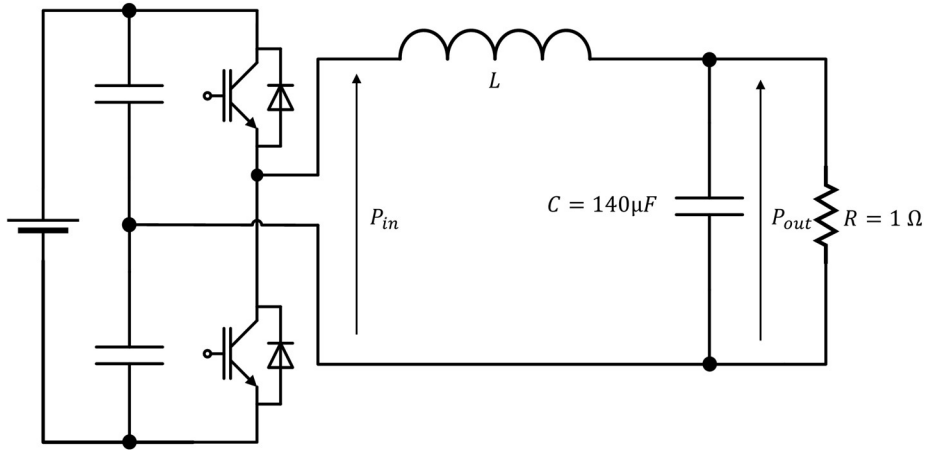


Fig. 15. Single-phase two-level inverter

The inductor voltage/current waveforms are captured and fed into the loss map to calculate the core loss. The resulting measured waveforms of the inductor voltage and current, and the load current are shown in Fig. 16 for one PWM operating point, where  $U_{DC}$  is the dc-link voltage;  $M$  is the modulation index;  $f_{sw}$  is the switching frequency;  $f_0$  is the fundamental frequency.

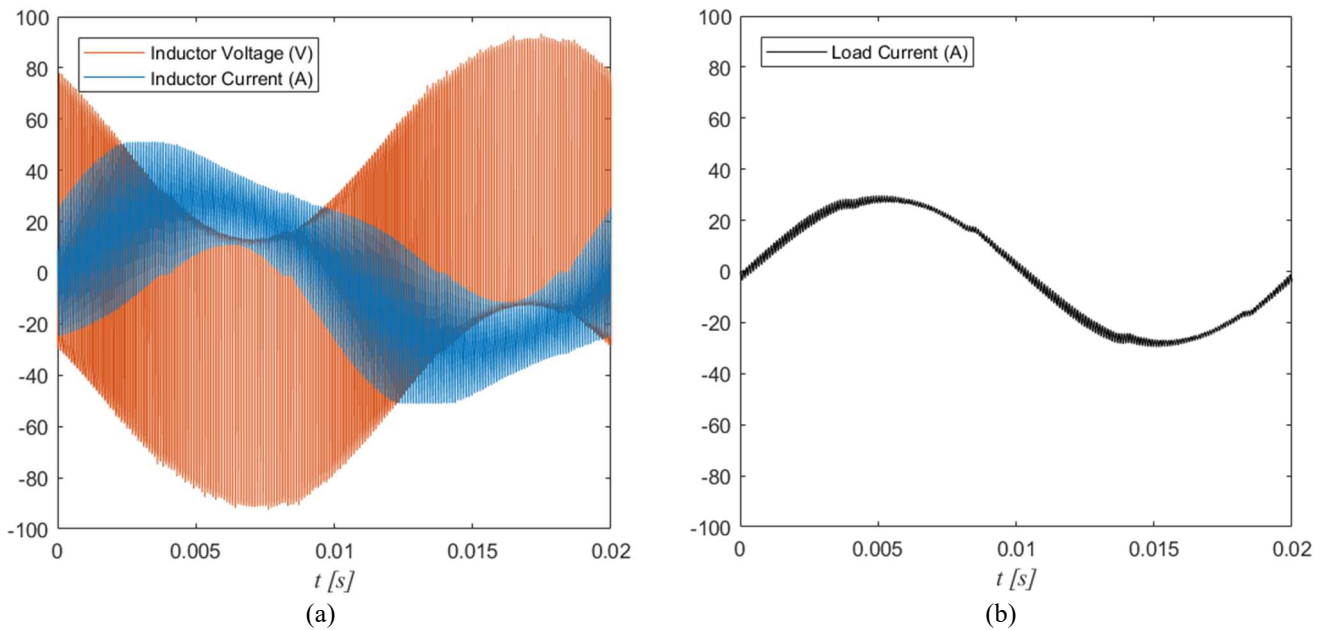


Fig. 16. Experimental waveforms (a) inductor voltage and current (b) filtered current in load resistor R  
 $U_{DC} = 100 \text{ V}$ ,  $M = 0.7$ ,  $f_{sw} = 10 \text{ kHz}$ ,  $f_0 = 50 \text{ Hz}$

The voltage/current information measured was fed through the calculation flow shown in Fig. 14 and the core loss for each segment is generated. The operating plane of the inductor described by the three variables is plotted in Fig. 17 over a fundamental cycle. In this case, the inductor voltage varies between 10 ~ 90 Volts; The volt-time product varies between 1000 to 2500 Volts-microseconds. The biased current is between -30 ~ +30 A, equals to the filtered fundamental-frequency load current. The core loss of each segments is calculable as the pre-built loss map covers the whole operating plane.

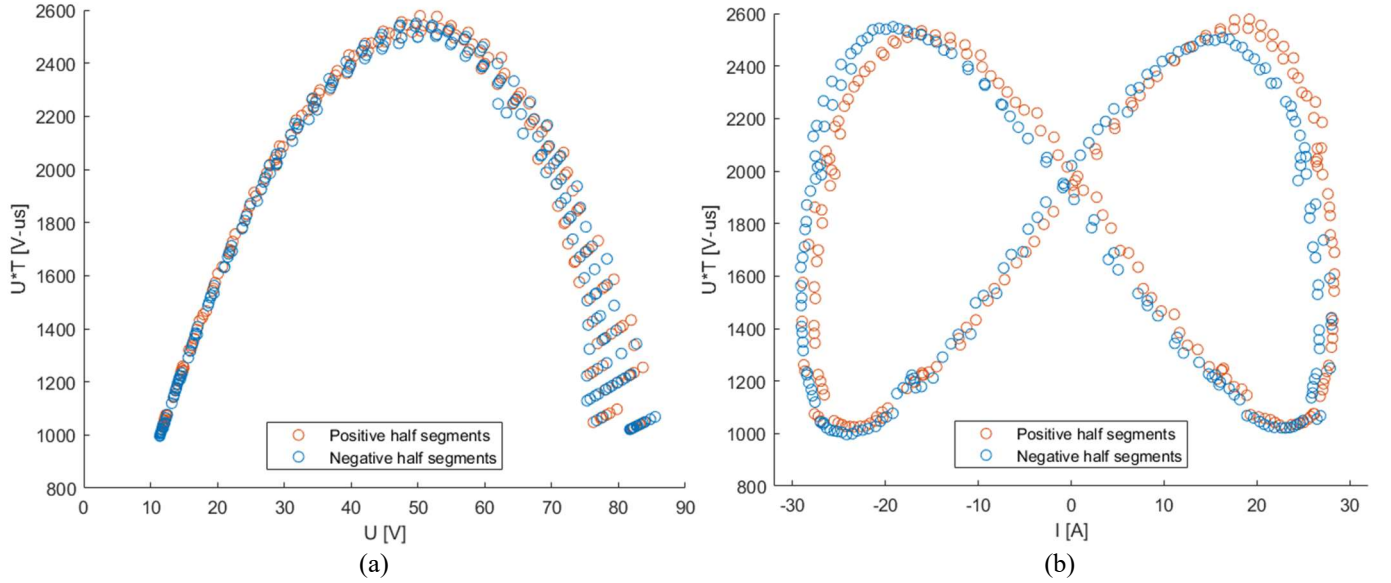


Fig. 17. Operating plane of the core (a)  $U \cdot T$  and  $U$  (b)  $U \cdot T$  and  $I$  ( $U_{DC} = 100$  V,  $M = 0.7$ ,  $f_{sw} = 10$  kHz)

Calculated from the loss map approach, the instantaneous core loss is shown in Fig. 18 over a fundamental cycle. As  $f_{sw} = 10$  kHz and  $f_0 = 50$  Hz, the instantaneous core loss of 400 positive half segments and 400 negative half segments are found and plotted in Fig. 18 (a). Within each switching cycle, the core loss of the positive half and negative half are added up to obtain the instantaneous core loss of each switching window, which is plotted in Fig. 18 (b). It can be seen that, for one fundamental sinusoidal cycle, there are two peaks of the core loss occurring at maximum inductor current ripple.

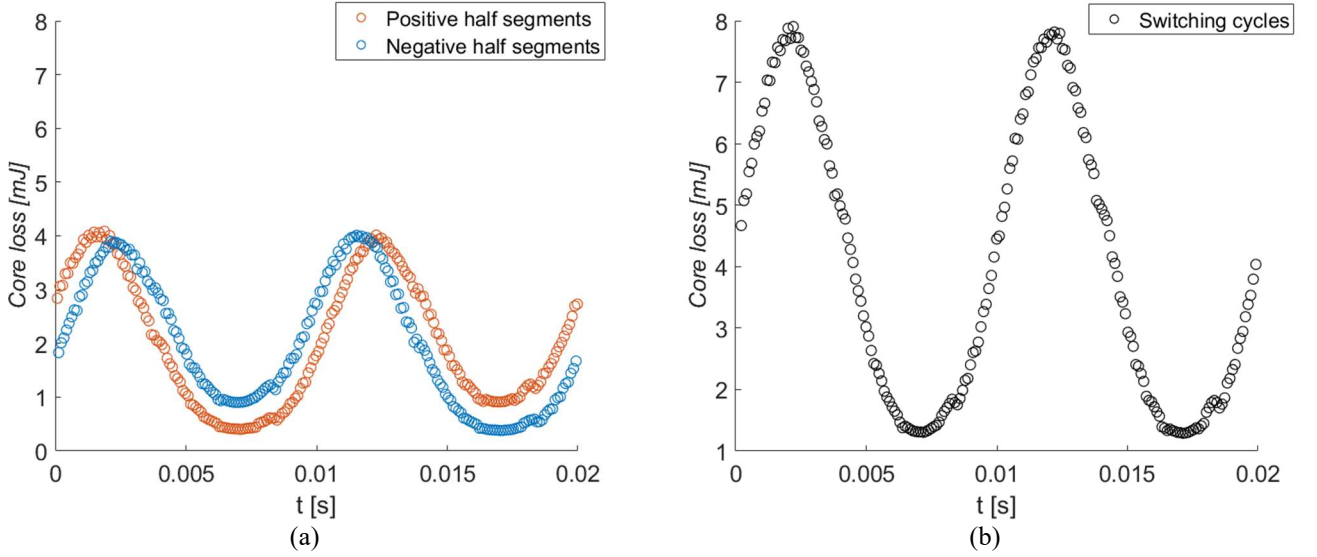


Fig. 18. Estimated core loss over one fundamental cycle (a) Plotted by half-loop segments (b) Plotted by switching cycles ( $U_{DC} = 100$  V,  $M = 0.7$ ,  $f_{sw} = 10$  kHz)

In addition to the core loss, the copper loss of the inductor can be estimated relatively accurately by analytical models. The dc resistance of the windings is measured by a dc milliohm meter of  $3.59$  m $\Omega$ . Considering both skin effect and proximity effect, the ac-to-dc resistance ratio of the rectangular winding selected at a particular frequency can be calculated by (20) [33].

$$F_R = \frac{R_{AC}}{R_{DC}} = \frac{h}{\delta} \eta \left[ \frac{\sinh\left(2\frac{h}{\delta}\right) + \sin\left(2\frac{h}{\delta}\right)}{\cosh\left(2\frac{h}{\delta}\right) - \cos\left(2\frac{h}{\delta}\right)} + \frac{2}{3}(N_l^2 - 1) \cdot \frac{\sinh\left(\frac{h}{\delta}\right) - \sin\left(\frac{h}{\delta}\right)}{\cosh\left(\frac{h}{\delta}\right) + \cos\left(\frac{h}{\delta}\right)} \right] \quad (20)$$

Where  $h$  is the thickness of the conductor;  $\delta$  is the skin depth;  $\eta$  is the porosity factor;  $N_l$  is the layer numbers. Note the windings of the inductor shown in Fig. 7 are stacked parallelly in the horizontal direction with regard to the centre of the cores. In this case the layer numbers equals to the turn number ( $N_l = 6$ ) according to [33]. The fringing flux effect on the windings is neglected, since the winding is spaced away from the central leg airgap. The measured inductor current is processed by Fast Fourier Transformation (FFT) in Matlab to extract the amplitude-frequency spectrum. For each frequency components, the ac resistance is calculated individually. Following equation (21), the total copper loss is obtained by adding up the copper losses for all the frequency components [33].

$$P_w = R_{wdc} I_0^2 + R_{wdc} \sum_{n=1}^{\infty} F_{Rn} I_n^2 \quad (21)$$

The total power loss of the inductor is experimentally measured according to (23) by measuring the input ( $P_{in}$ ) and output power ( $P_{out}$ ) of the inductor (shown in Fig. 15) with the power loss on the capacitor neglected. The powers are obtained by

mathematically integrating the instantaneous voltage-current product and averaging it over fundamental cycles, as in (22). The voltage and current signals are measured with the high-bandwidth voltage and current probes shown in Table III as in the TPT.

$$P = \frac{1}{2\pi} \int_0^{2\pi} U \cdot I \, d\theta \quad (22)$$

Rather than directly integrating the inductor voltage and current, the real power loss of the inductor is measured by  $P_{in} - P_{out}$  to reduce the error caused by the phase discrepancy of the probes. As demonstrated in [24], the greater power factor of a voltage-current pair has, the less error in the measured real power loss would be caused by the phase discrepancy.

$$P_L = P_{in} - P_{out} \quad (23)$$

The estimated inductor core loss using the approach proposed in this paper and the calculated copper loss according to (21) are added up and compared with the experimentally measured total loss of the inductor. The results are shown in Fig. 19, with several combinations of dc-link voltage and switching frequency. It can be seen that the measured total power loss agrees very well with the sum of the estimated core loss and copper loss, with an average error of less than 5%. The results indicate that the core loss estimation approach proposed in this paper is valid and accurate.

Note at the lower switching frequency, i.e. 10kHz, the core loss is higher due to larger swings of flux density  $\Delta B$  of half-loop segments, which is proportional to volt-time product  $U_L \cdot T$ . Although the number of segments is doubled at 20 kHz, the larger  $\Delta B$  ( $U_L \cdot T$ ) of the segments in the 10 kHz case resulted in overall higher core loss.

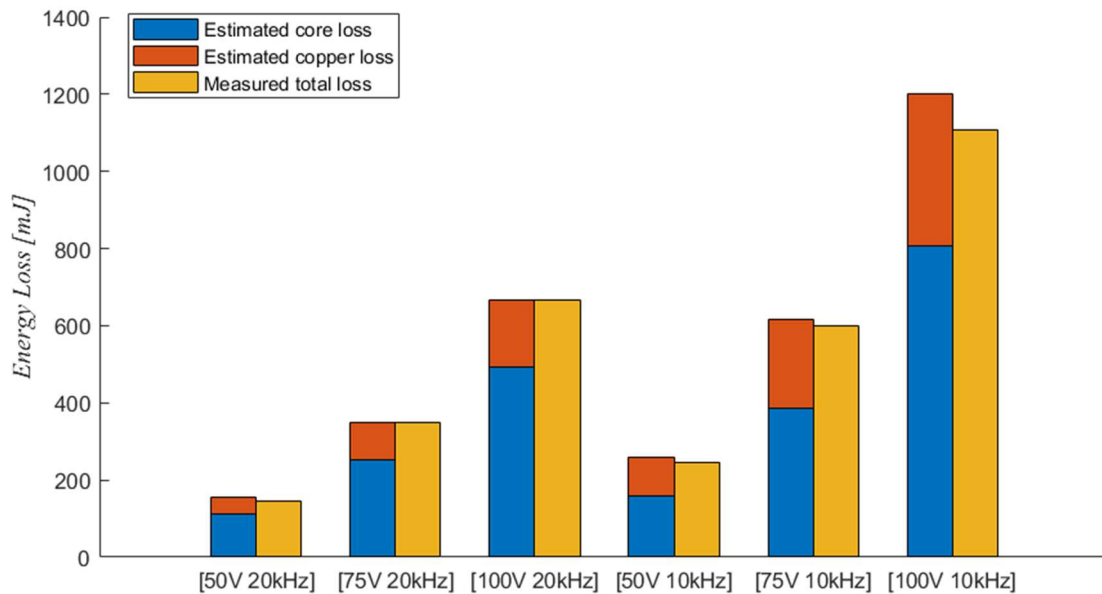


Fig. 19. Experimental results of inductor losses over one fundamental cycle (0.02 s) with various combinations of  $U_{DC}$  and  $f_{sw}$

## V. CONCLUSION

This paper has presented a whole process to characterise the core loss of a customised, high-current, gapped inductor and estimate its core loss for PWM operations. To overcome the challenges raised by high excitation current, a test circuit based on a half-bridge structure has been proposed and a Triple Pulse Test procedure was applied in the B-H loop measurement. The half-bridge converter configuration mitigates the asymmetric rectangular voltage across the inductor-under-test caused by device voltage drops. The Triple Pulse Test procedure reduces the requirements of the test setup (thermal stress, current-time stress for current probes, current capacity of dc sources, etc.) and enables a fast evaluation. For practical purposes, a user-friendly loss map and core loss calculation involving only time-domain and electrical variables have been proposed to enable a more straightforward loss mapping process and simplified core loss estimations. The loss map presented in the form of 2-D curves can be printed on manufacturer's datasheet of inductors. The proposed user-friendly loss map approach has been applied and verified in a single-phase two-level PWM converter, which validates the practicality and accuracy of the proposed approach.

It is anticipated that the manufacturers can perform out-of-factory tests on each single inductor or each batch of inductors with the same cores, rather than the core material, to establish the user-friendly core loss profile. Alternatively, the core loss map can be rapidly constructed on the user's side through the presented approach. The established core loss profiles will be beneficial for the users of inductors (e.g. power electronics engineers) to accurately predict the core loss in the design of PWM converters.

## ACKNOWLEDGEMENT

The authors would like to thank Prof. Toshihisa Shimizu for sharing insights and kind suggestions on this topic.

## REFERENCES

- [1] G. Calderon-Lopez, A. J. Forsyth, D. L. Gordon, and J. R. McIntosh, "Evaluation of SiC BJTs for High-Power DC-DC Converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2474–2481, Jul. 2014.
- [2] R. M. Burkart, H. Uemura, and J. W. Kolar, "Optimal inductor design for 3-phase voltage-source PWM converters considering different magnetic materials and a wide switching frequency range," *Proc. International Power Electronics Conf.*, 2014, pp. 891–898.
- [3] J. W. Kolar *et al.*, "PWM converter power density barriers," in *Proc. Power Conversion Conf.*, 2007, pp. 9–29.
- [4] H. Uemura, F. Krismer, Y. Okuma, and J. W. Kolar, "η-p Pareto Optimization of 3-Phase 3-Level T-type AC-DC-AC Converter Comprising Si and SiC Hybrid Power Stage," in *Proc. International Power Electronics Conf.*, 2014, pp. 2834–2841.
- [5] C. R. Sullivan and J. H. Harris. (2010). Testing Core Loss for Rectangular Waveforms, Phase II Final Report. [Online].



Available: <http://www.psmma.com/coreloss/phase2.pdf>

- [6] S. Iyasu, T. Shimizu, and K. Ishii, "A novel iron loss calculation method on power converters based on dynamic minor loop," in *Proc. European Conference on Power Electronics and Applications*, 2005, pp. 2016–2022.
- [7] K. Terashima, K. Wada, T. Shimizu, T. Nakazawa, K. Ishii, and Y. Hayashi, "Evaluation of the iron loss of an inductor based on dynamic minor characteristics," *Proc. European Conf. on Power Electronics and Applications*, 2007, pp. 1–8.
- [8] T. Shimizu and S. Iyasu, "A practical iron loss calculation for AC filter inductors used in PWM inverters," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 7, pp. 2600–2609, Apr. 2009.
- [9] J. Muhlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Core losses under the DC bias condition based on steinmetz parameters," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 953–963, Jun. 2012.
- [10] C. R. Sullivan, "High frequency core and winding loss modeling," in *Proc. IEEE International Electric Machines and Drives Conf.*, 2013, pp. 1482–1499.
- [11] C. R. Sullivan and J. H. Harris. (2010) Testing Core Loss for Rectangular Waveforms. [Online]. Available: <http://www.psmma.com/coreloss/pilot.pdf>
- [12] J. Reinert, A. Brockmeyer, and R. W. A. A. De Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified Steinmetz equation," *IEEE Transactions on Industry Applications*, vol. 37, no. 4, pp. 1055–1061, Aug. 2001.
- [13] J. Li, T. Abdallah, and C. R. Sullivan, "Improved Calculation of Core Loss with Nonsinusoidal Waveforms," in *Proc. Industry Applications Conf.*, 2001, pp. 2203–2210.
- [14] K. Venkatachalani, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate Prediction of Ferrite Core Loss with Nonsinusoidal Waveforms Using Only Steinmetz Parameters," in *Proc. IEEE Workshop on Computers in Power Electronics*, 2002, pp. 36–41.
- [15] H. Matsumori, T. Shimizu, K. Takano, and H. Ishii, "Evaluation of iron loss of AC filter inductor used in three-phase PWM inverters based on an iron loss analyzer," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 3080–3095, Jul. 2016.
- [16] H. Matsumori, T. Shimizu, K. Takano, and H. Ishii, "Novel iron loss calculation model for AC filter inductor on PWM inverter," in *Proc. IEEE International Power Electronics and Motion Control Conf.*, 2016, pp. 3676–3681.
- [17] T. Shimizu, K. Kakazu, H. Matsumori, K. Takano, and H. Ishii, "Iron loss evaluation of filter inductor used in PWM inverters," in *Proc. IEEE Energy Conversion Congress and Exposition*, 2011, pp. 606–613.
- [18] Y. Wang, G. Calderon-Lopez, and A. Forsyth, "High Frequency Gap Losses in Nanocrystalline Cores," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4683–4690, Aug. 2016.
- [19] W. Shen, F. Wang, D. Boroyevich, and C. W. Tipton IV, "High-density nanocrystalline core transformer for high-power high-frequency resonant converter," *IEEE Transactions on Industry Applications*, vol. 44, no. 1, pp. 213–222, Jan. 2008.
- [20] J. Muhlethaler, "Modeling and Multi-Objective Optimization of Inductive Power Components," PhD thesis, ETH Zurich, 2012.
- [21] E. Herbert. (2012). Testing Core Loss for Rectangular Waveforms, Phase II Supplemental Report. [Online]. Available: <http://www.psmma.com/coreloss/supplement.pdf>
- [22] H. Matsumori, T. Shimizu, X. Wang, and F. Blaabjerg, "A Practical Core Loss Model for Filter Inductors of Power Electronic Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 1, pp. 29–39, Oct. 2018.
- [23] K. Umetani, "Improvement of saturation property of iron powder core by flux homogenizing structure," *IEEE Transactions on Electrical and Electronic Engineering*, vol. 8, no. 6, pp. 640–648, 2013.

- [24] M. Mu, Q. Li, D. J. Gilham, F. C. Lee, and K. D. T. Ngo, "New core loss measurement method for high-frequency magnetic materials," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4374–4381, Oct. 2014.
- [25] J. Mühlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Improved core-loss calculation for magnetic components employed in power electronic systems," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 964–973, Jul. 2012.
- [26] C. R. Sullivan, J. H. Harris, and E. Herbert, "Core loss predictions for general PWM waveforms from a simplified set of measured data," in *Proc. Applied Power Electronics Conference and Exposition*, 2010, pp. 1048–1055.
- [27] I. Laird, X. Yuan, J. Scoltock, and A. Forsyth, "A Design Optimisation Tool for Maximising the Power Density of 3-Phase DC-AC Converters Using Silicon Carbide (SiC) Devices," *IEEE Transactions on Power Electronics*, vol. 33, no. 4, pp. 2913–2932, May 2017.
- [28] J. Muhlethaler, J. Biela, A. Ecklebe, and J. W. Kolar, "Improved Core-Loss Calculation for Magnetic Components Employed in Power Electronic Systems," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 964–973, Jul. 2012.
- [29] G. Niedermeier and M. Esguerra, "Measurement of Power Losses with DC-Bias – The Displacement Factor," in *Proc. International Conference on Power Conversion/Intelligent Motion*, 2000, pp. 169–174.
- [30] H. Matsumori, T. Shimizu, K. Takano, and H. Ishii, "Iron loss calculation of AC filter inductor for three-phase PWM inverter," in *Proc. IEEE Energy Conversion Congress and Exposition*, 2015, pp. 3049–3056.
- [31] J. H. Harris. (2013). Testing Core Loss for Rectangular Waveforms, Phase III Final Report. [Online]. Available: <http://www.pσμα.com/sites/default/files/uploads/files/p3dartmouthrpt1.pdf>
- [32] E. Herbert. (2013). Testing Core Loss for Rectangular Waveforms, Phase III Supplemental Report: The String of Beads Experiment. [Online]. Available: <http://www.pσμα.com/sites/default/files/uploads/files/p3suprpt1.pdf>
- [33] K. K. Marian, *High-Frequency Magnetic Components*, 2nd ed. Chichester: WILEY, 2014.